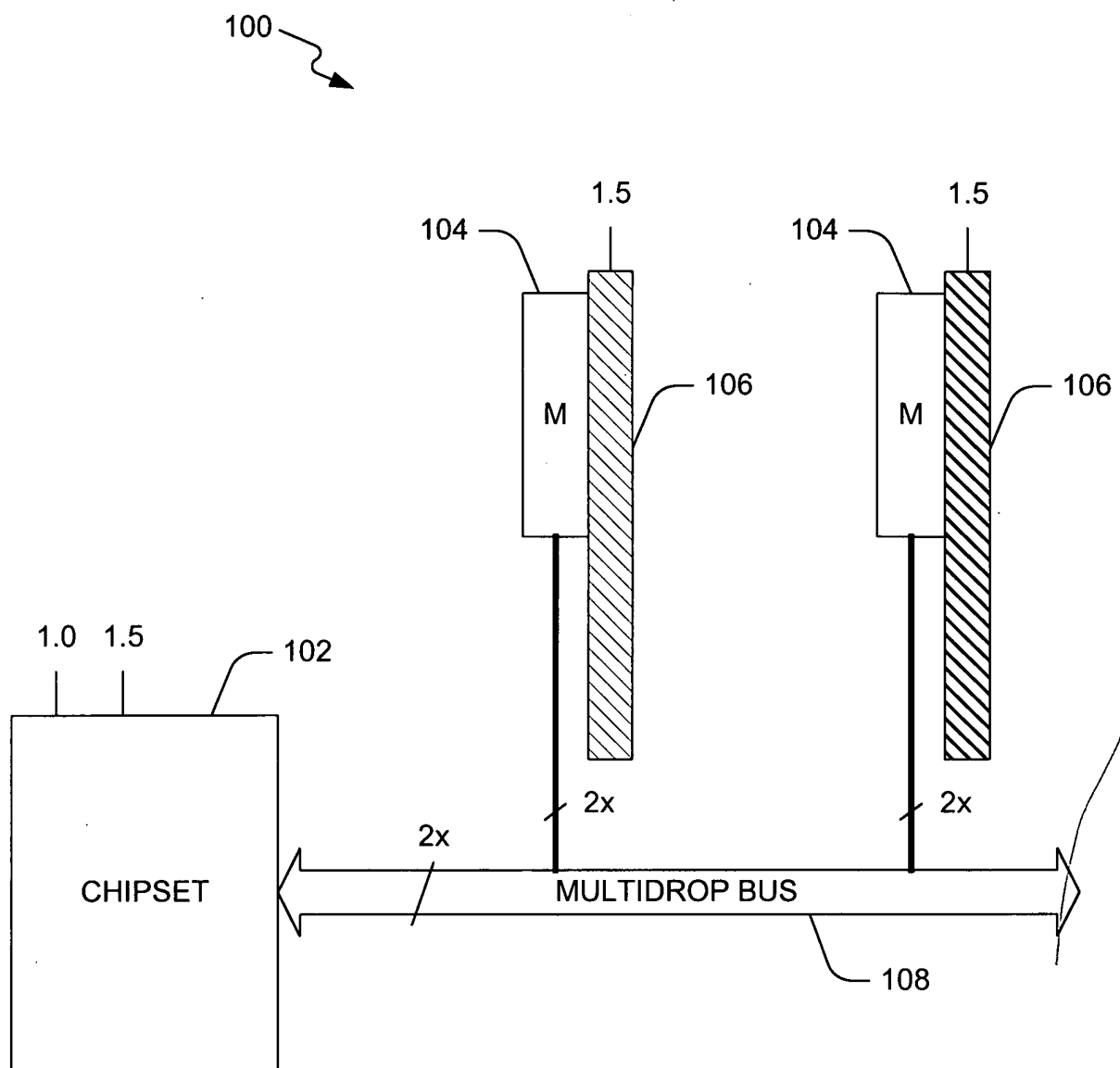
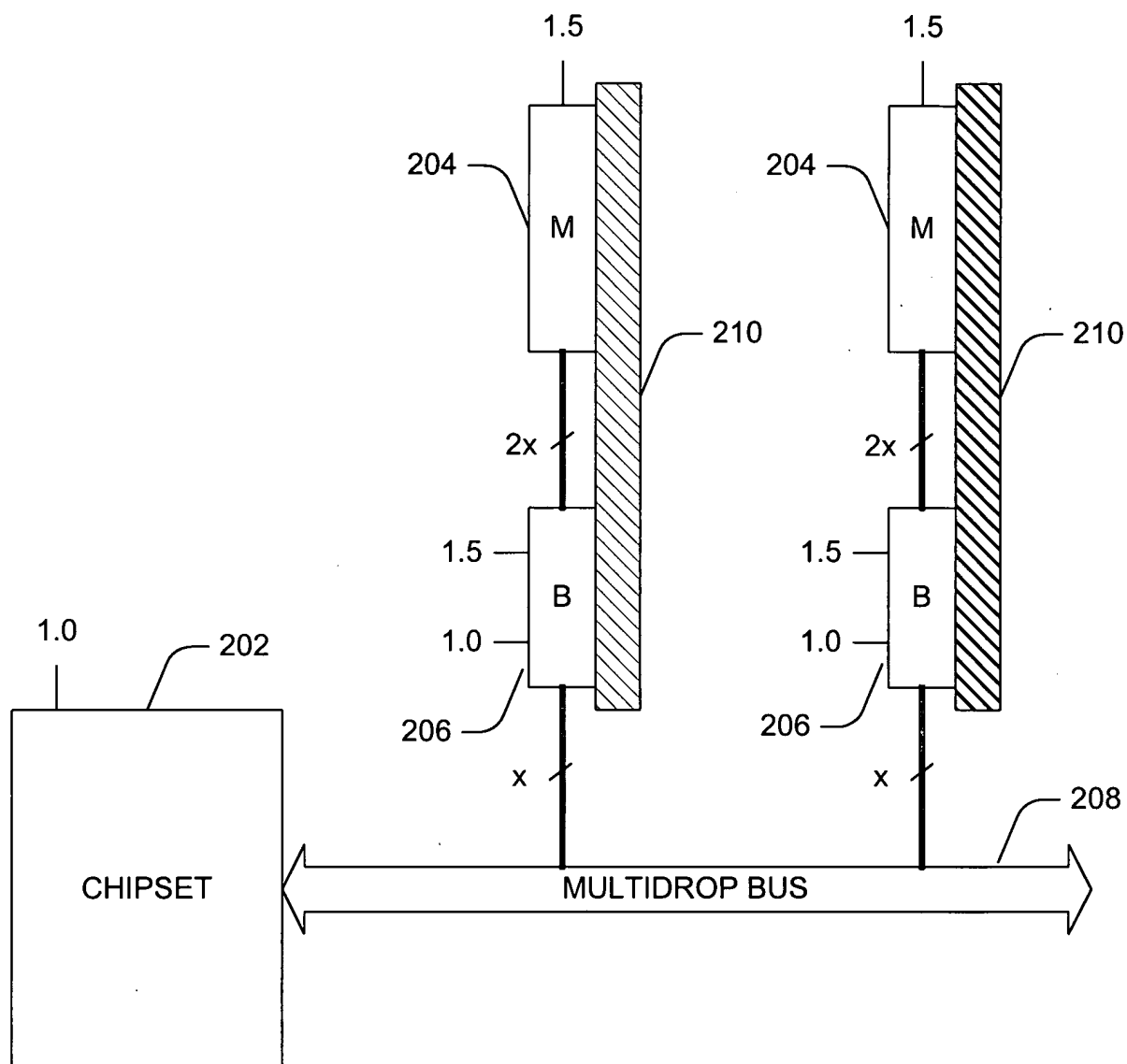


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**FIG. 1**  
**(PRIOR ART)**

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**FIG. 2**



The diagram illustrates a dual-channel memory architecture. On the left, a block labeled 408 represents the CHIPSET. Two horizontal buses extend from the chipset: an ADDRESS BUS and a DATA BUS. Two memory channels are connected to these buses. Each channel is enclosed in a large rectangle. Inside each channel, there are four memory modules (labeled 406) at the top. Below the modules is an ADDRESS/COMMAND block, and below that are two DATA BUFFER blocks. The ADDRESS BUS connects to the ADDRESS/COMMAND blocks in both channels. The DATA BUS connects to the DATA BUFFER blocks in both channels. Arrows indicate the direction of data flow between the modules, buffers, and the external buses.

**FIG. 4**

START

PROVIDING A PLURALITY OF BUFFERS IN AN INTERFACE BETWEEN A CHIPSET AND MEMORY MODULES. THE BUFFERS ALLOWING THE MEMORY INTERFACE TO BE SPLIT INTO TWO INTERFACES. THE FIRST INTERFACE FORMED BETWEEN THE CHIPSET AND THE BUFFERS. THE SECOND INTERFACE FORMED BETWEEN THE BUFFERS AND THE MEMORY MODULES.

500

CONFIGURING THE PLURALITY OF BUFFERS TO PROPERLY LATCH THE DATA TRANSFERED BETWEEN THE CHIPSET AND THE MEMORY MODULES SUCH THAT THE TWO INTERFACES OPERATE INDEPENDENTLY BUT IN SYNC WITH EACH OTHER

502

END

**FIG. 5**